REMARKS

This application has been carefully reviewed in light of the Office Action dated December 19, 2003. Applicant has amended claims 1 and 7 and has added claim 15. Reconsideration and favorable action in this case are respectfully requested.

The Examiner has rejected claims 1-3, 5-11, 13 and 14 under 35 U.S.C. §102(b) as being unpatentable over U.S. Pat. No. 5,920,353 to Diaz et al (hereinafter "Diaz"). Applicants have reviewed this reference in detail and do not believe that it discloses or makes obvious the invention as claimed.

The Examiner has also rejected claims 4 and 12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 5,920,353 to Diaz and U.S. Pat. No. 5,790,208 to Kwak. Applicants have reviewed these references in detail and do not believe that they disclose or make obvious the invention as claimed.

The present invention as defined by claim 1 is directed to circuitry for processing images and video, where a processor executes software instructions for processing images and video and certain instructions relating to motion estimation and transform coding cause the processor to send a request to a motion estimation hardware accelerator or a transform coding hardware accelerator, which then processes data from the random access memory and sends a result to the processor. The processor then further processes the video or image based on the received results.

Applicants have reviewed the Diaz reference in detail, and particularly the sections cited by the Examiner. It is clear from Diaz that the decoder 200, as shown in Figures 2 and 3, is a stand-alone decoder. As noted by the Examiner, if the decoder is to be used with a processor 75, certain functions in the decoder could be performed by the processor 75. By removing functions from the decoder and using the processor 75 to perform these functions, the size of the die for the decoder could be reduced (col. 9, lines 39-52). The

functions that could be performed by the processor 75, as noted by the Examiner, include controlling the encoder module 88 (col. 9, lines 34-37), portions of motion estimation (col 8, lines 5-15), and operating as a multiplexer (column 9, lines 30-33).

However, none of the passages cited by the Examiner teach what is claimed in claim 1 – namely, that video or image processing is performed by executing software instructions in the processor, where the processor requests motion estimations to be performed by a motion estimation hardware accelerator and where the processor requests transform coding functions to be performed by a transform coding hardware accelerator, and where, responsive to a request, each hardware accelerator operates on data from the random access memory and returns a result to the processor, such that the processor can continue processing the video or image.

There is nothing in Diaz to suggest that the processor, if used to perform a function block from the decoder 200, is sending requests to hardware in the decoder in response to software instructions that could benefit from a hardware accelerator. There is nothing to suggest that the processor receives a result from a hardware accelerator in the decoder and further processes a video or image based on the result. Diaz only teaches that in order to make a smaller die for the decoder 200, some functions can be performed by a processor.

Accordingly, Applicant respectfully requests allowance of claim 1 and dependent claims 2-7. For reasons discussed in connection with claim 1, Applicant also respectfully requests allowance of claim 7 and dependent claims 8-14.

Applicant has also added claim 15. As discussed in the present specification on page 31, first paragraph, the execution of code in the hardware accelerators can be dynamically configured in real time – certain instructions can be processed in an accelerator, if present; if not present, the processor can process the instruction.

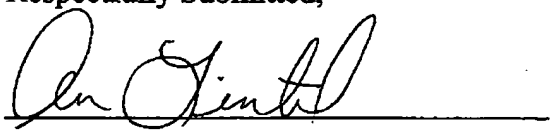
This aspect of the invention allows for a single program to be written for a video processing application, without previous knowledge of whether the accelerators will be present on the target device.

The Commissioner is hereby authorized to charge any fees or credit any overpayment, including extension fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Alan W. Lintel, Applicants' Attorney at (972) 664-9595 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



Alan W. Lintel
Attorney for Applicant(s)
Reg. No. 32478

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Anderson, Levine & Lintel
14785 Preston Rd.
Suite 650
Dallas, Texas 75254
Tel. (972) 664-9595